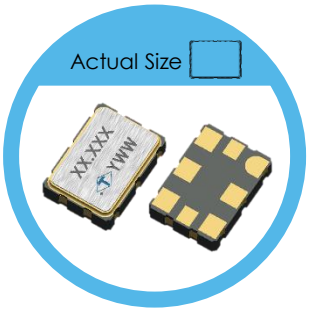
TAITIEN
Our Performance, Your Reputation

VD-M Type High Frequency & Ultra Low Noise
7.0 x 5.0 mm Differential Output Voltage Controlled Crystal Oscillator



RoHS Compliant

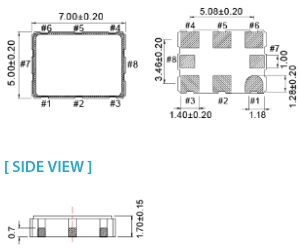
FEATURES

- Pb-free/RoHS Compliant
- Tri-state Enable / Disable Mode
- Temperature Range: -40 to 85 ˚C
- Clock Output: LVPECL, LVDS, CML, HCSL and CMOS
- Output Frequency Support from 15MHz to 2.1GHz
- Low Power Supply Voltage: 3.3, 2.5, and 1.8V Supply Options
- Ultra Low Phase RMS jitter: Typical: 250fs at 12kHz to 20MHz Frequency Offsets

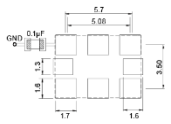
TYPICAL APPLICATION

- Set-Top Box, HDTV
- xDSL/VoIP, Cable Modem
- Jitter Attenuator, ADC

DIMENSION (mm)

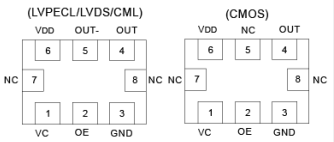


SOLDER PAD LAYOUT (mm)



Please ensure optimal oscillator performance, place a by-pass capacitor of 0.1µF as close to the part as possible between V_{DD} and GND pads

PIN ASSIGNMENTS



PIN FUNCTION (mm)

PIN#	FUNCTION	
	LVPECL/LVDS/CML	CMOS
1	V_{con}	V_{con}
2	OE	OE
3	GND	GND
4	Output	Output
5	Comp. Output	NC
6	V_{DD}	V_{DD}
7	NC	NC
8	NC	NC

ELECTRICAL SPECIFICATION

Parameter		LVPECL 3.3V Min.	LVPECL 3.3V Max.	LVPECL 2.5V Min.	LVPECL 2.5V Max.	Unit	Test Condition
Supply Voltage Variation (V_{DD})		2.97	3.63	2.25	2.75	V	
Frequency Range		15	2100	15	2100	MHz	
Supply Current			120		95	mA	
Output Level	Output High	V_{DD} – 1.165	V_{DD} – 0.8	V_{DD} – 1.165	V_{DD} – 0.8	V	
	Output Low	V_{DD} – 2.0	V_{DD} – 1.55	V_{DD} – 2.0	V_{DD} – 1.55	V	
Transition Time (20% – 80%)	Rise Time		0.35		0.35	nSec	
	Fall Time		0.35		0.35	nSec	
Duty Cycle		45	55	45	55	%	
Startup Time			8		8	mSec	
Tri-State Mode (Input to Pin 2)	Enable	0.7 x V_{DD}		0.7 x V_{DD}		V	
	Disable		0.3 x V_{DD}		0.3 x V_{DD}	V	
Stand by Current			120		95	mA	
Output Load		50Ω into V_{DD} – 2V					
Phase Noise		Typ.	Max.	Typ.	Max.		
At V_{DD}=3.3V, fout=644.5MHz	1kHz offset	-87		-87		dBc/Hz	
	10kHz offset	-110		-110		dBc/Hz	
	100kHz offset	-127		-127		dBc/Hz	
	1MHz offset	-138		-138		dBc/Hz	
	20MHz offset	-153		-153		dBc/Hz	
RMS Phase Jitter (Integrated 12 kHz~20 MHz)		250	300	250	300	fs	
Period Jitter			50		50	ps	

Note: not all combination of options are available. Other specifications may be available upon request.

Specifications subject to change without notice.

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Parameter		LVDS						Unit	Test Condition
		3.3V		2.5V		1.8V			
		Min.	Max.	Min.	Max.	Min.	Max.		
Supply Voltage Variation (V_{DD}) ±10%		2.97	3.63	2.25	2.75	1.71	1.89	V	
Frequency Range		15	2100	15	2100	15	2100	MHz	
Supply Current			90		80		70	mA	
Output Level	Output High		1.6		1.6		1.6	V	
	Output Low	0.9		0.9		0.9		V	
Transition Time (20% – 80%)	Rise Time		0.35		0.35		0.35	nSec	
	Fall Time		0.35		0.35		0.35	nSec	
Duty Cycle		45	55	45	55	45	55	%	
Startup Time			8		8		8	mSec	
Tri-State Mode	Enable	0.7 x V_{DD}		0.7 x V_{DD}		0.7 x V_{DD}		V	
(Input to Pin 2)	Disable		0.3 x V_{DD}		0.3 x V_{DD}		0.3 x V_{DD}	V	
Stand by Current			90		80		70	mA	
Output Load		100Ω (Between OUT & OUTN)							
Phase Noise		Typ.	Max.	Typ.	Max.	Typ.	Max.		
At V_{DD}=3.3V, fout=644.5MHz	1kHz offset	-87		-87		-87		dBc/Hz	
	10kHz offset	-110		-110		-110		dBc/Hz	
	100kHz offset	-127		-127		-127		dBc/Hz	
	1MHz offset	-138		-138		-138		dBc/Hz	
	20MHz offset	-153		-153		-153		dBc/Hz	
RMS Phase Jitter (Integrated 12 kHz~20 MHz)		250	300	250	300	250	300	fs	
Period Jitter			50		50		50	ps	

Parameter		HCSL						Unit	Test Condition
		3.3V		2.5V		1.8V			
		Min.	Max.	Min.	Max.	Min.	Max.		
Supply Voltage Variation (V_{DD})		2.97	3.63	2.25	2.75	1.71	1.89	V	
Frequency Range		15	700	15	700	15	700	MHz	
Supply Current			115		100		94	mA	
Output Level	Output High	0.66	1.15	0.66	1.15	0.66	1.15	V	
	Output Low	0	0.15	0	0.15	0	0.15	V	
Transition Time (20% – 80%)	Rise Time		0.4		0.4		0.4	nSec	
	Fall Time		0.4		0.4		0.4	nSec	
Duty Cycle		45	55	45	55	45	55	%	
Startup Time			8		8		8	mSec	
Tri-State Mode	Enable	0.7 x V_{DD}		0.7 x V_{DD}		0.7 x V_{DD}		V	
(Input to Pin 2)	Disable		0.3 x V_{DD}		0.3 x V_{DD}		0.3 x V_{DD}	V	
Stand by Current			115		100		94	mA	
Output Load		50Ω to GND							
Phase Noise		Typ.	Max.	Typ.	Max.	Typ.	Max.		
At V_{DD}=3.3V, fout=644.5MHz	1kHz offset	-87		-87		-87		dBc/Hz	
	10kHz offset	-110		-110		-110		dBc/Hz	
	100kHz offset	-127		-127		-127		dBc/Hz	
	1MHz offset	-138		-138		-138		dBc/Hz	
	20MHz offset	-153		-153		-153		dBc/Hz	
RMS Phase Jitter (Integrated 12 kHz~20 MHz)		250	300	250	300	250	300	fs	
Period Jitter			50		50		50	ps	

Parameter		CML						Unit	Test Condition
		3.3V		2.5V		1.8V			
		Min.	Max.	Min.	Max.	Min.	Max.		
Supply Voltage Variation (V_{DD})		2.97	3.63	2.25	2.75	1.71	1.89	V	
Frequency Range		15	2100	15	2100	15	2100	MHz	
Supply Current			90		80		70	mA	
Output Level	Output High	V_{DD} – 0.085	V_{DD}	V_{DD} – 0.085	V_{DD}	V_{DD} – 0.085	V_{DD}	V	
	Output Low	V_{DD} – 0.6	V_{DD} – 0.32	V_{DD} – 0.6	V_{DD} – 0.32	V_{DD} – 0.6	V_{DD} – 0.32	V	
Transition Time (20% – 80%)	Rise Time		0.35		0.35		0.35	nSec	
	Fall Time		0.35		0.35		0.35	nSec	
Duty Cycle		45	55	45	55	45	55	%	
Startup Time			8		8		8	mSec	
Tri-State Mode	Enable	0.7 x V_{DD}		0.7 x V_{DD}		0.7 x V_{DD}		V	
(Input to Pin 2)	Disable		0.3 x V_{DD}		0.3 x V_{DD}		0.3 x V_{DD}	V	
Stand by Current			90		80		70	mA	
Output Load		50Ω to V_{DD}							
Phase Noise		Typ.	Max.	Typ.	Max.	Typ.	Max.		
At V_{DD}=3.3V, fout=644.5MHz	1kHz offset	-87		-87		-87		dBc/Hz	
	10kHz offset	-110		-110		-110		dBc/Hz	
	100kHz offset	-127		-127		-127		dBc/Hz	
	1MHz offset	-138		-138		-138		dBc/Hz	
	20MHz offset	-153		-153		-153		dBc/Hz	
RMS Phase Jitter (Integrated 12 kHz~20 MHz)		250	300	250	300	250	300	fs	
Period Jitter			50		50		50	ps	

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Parameter		CMOS						Unit	Test Condition
		3.3V		2.5V		1.8V			
		Min.	Max.	Min.	Max.	Min.	Max.		
Supply Voltage Variation (V_{DD})		2.97	3.63	2.25	2.75	1.71	1.89	V	
Frequency Range		15	250	15	250	15	250	MHz	
Supply Current			90		80		70	mA	
Output Level	Output High	0.9 x V_{DD}		0.9 x V_{DD}		0.9 x V_{DD}		V	
	Output Low		0.1 x V_{DD}		0.1 x V_{DD}		0.1 x V_{DD}	V	
Transition Time (20% – 80%)	Rise Time		1.2		1.5		2	nSec	
	Fall Time		1.2		1.5		2	nSec	
Duty Cycle	Fout<100MHz	45	55	45	55	45	55	%	
	Fout>100MHz	40	60	40	60	40	60	%	
Startup Time			8		8		8	mSec	
Tri-State Mode (Input to Pin 2)	Enable	0.7 x V_{DD}		0.7 x V_{DD}		0.7 x V_{DD}		V	
	Disable		0.3 x V_{DD}		0.3 x V_{DD}		0.3 x V_{DD}	V	
Stand by Current			90		80		70	mA	
Output Load		15pF							
Period Jitter			100		100		100	ps	

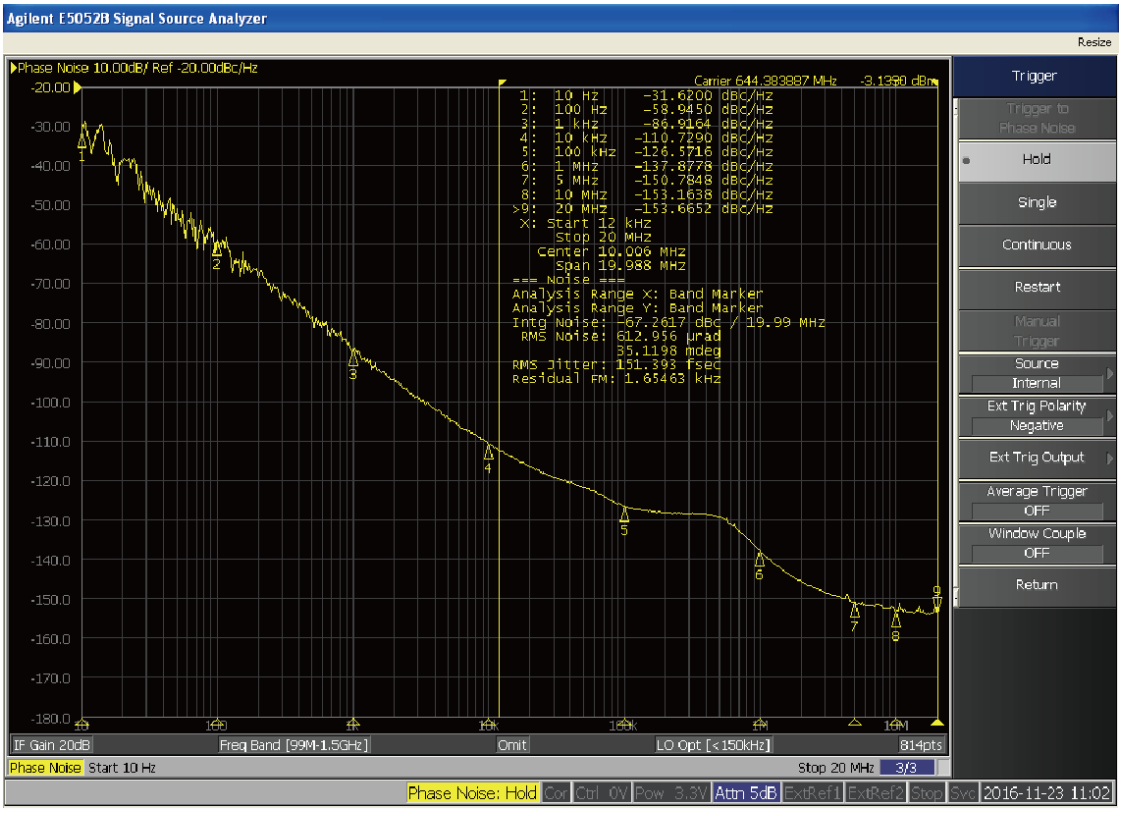
CONTROL VOLTAGE FUNCTION

Parameter	Control Voltage Function on Pin 1						Unit	Test Condition
	3.3V		2.5V		1.8V			
	Min.	Max.	Min.	Max.	Min.	Max.		
Control Voltage Center	1.65		1.25		0.9		V	
Control Voltage Range	0.3	3	0.25	2.25	0.18	1.62	V	
Frequency Pulling Range	±50	±250	±50	±250	±50	±250	ppm	
Linearity		±10		±10		±10	%	
Modulation Bandwidth	5	20	5	20	5	20	KHz	
VC Input Impedance	5		5		5		MΩ	

FREQ. STABILITY vs. TEMP. RANGE

ppm / Temp.(°C)	±20	±25	±30	±50
-10 ~ +60	○	○	○	○
-20 ~ +70	△	○	○	○
-40 ~ +85	×	○	○	○

○: Available △:Conditional ×: Not Available
Inclusive of calibration @ 25°C ,operating temperature rrange,input Voltage variation,load variation,aging (1st year),shock,and vibration



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