Application Notes:
PECL and LVDS Outputs

What are PECL and LVPECL?

- PECL stands for “Positive Emitter Coupled Logic”. PECL are differential logic outputs commonly used in high-speed clock distribution circuits. PECL requires a +5 V supply .

- Low Voltage PECL (LVPECL) denotes PECL circuits designed for use with 3.3V or 2.5V supply, the same supply voltage as for low voltage CMOS devices.

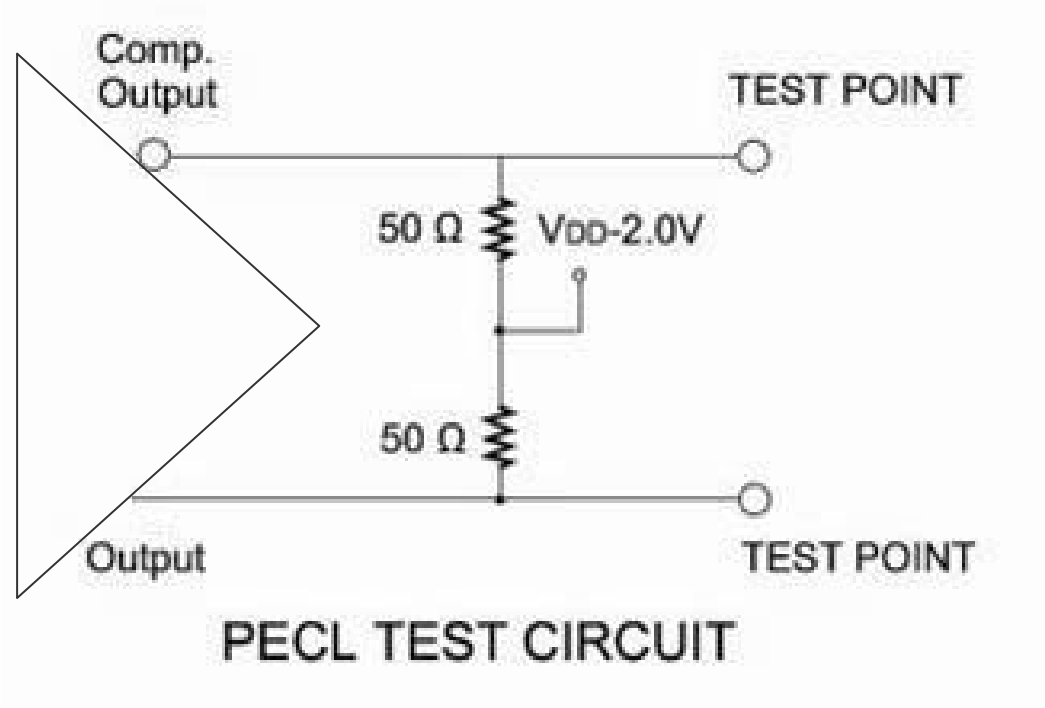
- Taitien offers LVPECL output crystal oscillators in both 3.3V and 2.5V supplies

Pros/Cons of PECL Output

- Advantages:
  - Very good jitter performance due to large voltage swing
  - Ideal use in high-speed circuits
  - Capable of driving long transmission lines

- Drawbacks:
  - Larger power consumption due to differential output and external DC biasing compared to single-ended output
  - Incompatible with 1.8V supply

Recommended PECL Termination Circuit



PECL TEST CIRCUIT

Each output is terminated with a 50Ω resistor to a termination voltage of (Vdd – 2V).

What is LVDS Output?

- LVDS stands for Low Voltage Differential Signaling, centered around operating voltage of 1.2V, regardless of power supply.

- LVDS technology is defined by the ANSI/TIA/EIA-644 industry standard.

- Taitien has many crystal oscillator product lines with LVDS output options at 3.3V and 2.5V supplies.

Pros/Cons of LVDS Output

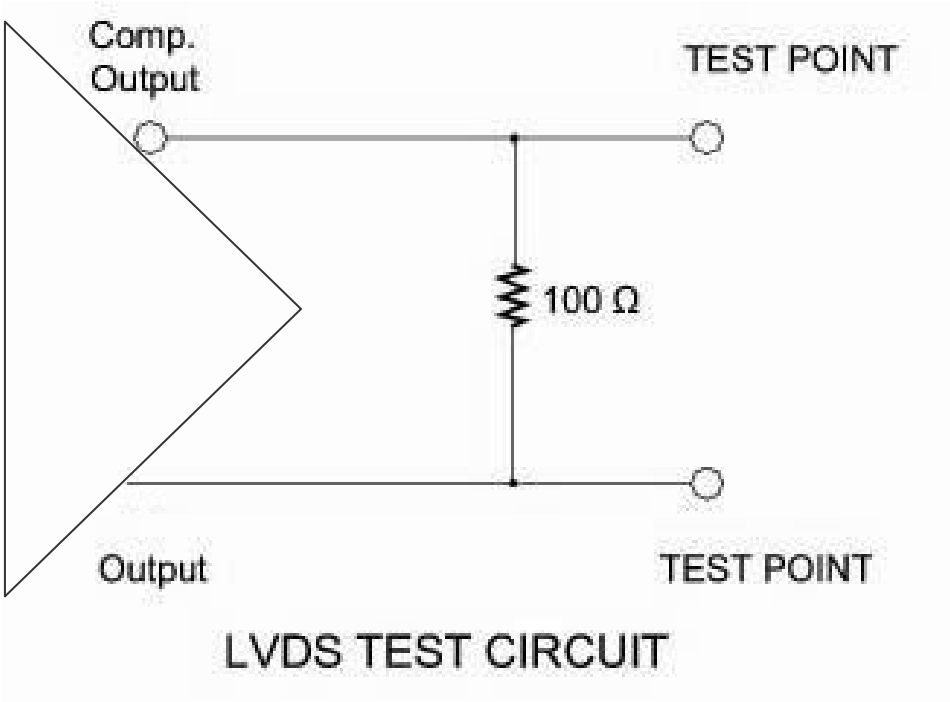
- Advantages:
  - Lower power consumption compared to PECL outputs due to smaller voltage swings (typically ~350mV)
  - Less susceptible to noise
  - Lower EMI emissions compared to CMOS/TTL

- Drawbacks:
  - Reduced jitter performance compared to PECL

Where is LVDS used?

The LVDS standard was created to address applications in the data communications, telecommunications, server, peripheral and computer markets where high-speed data transfer is necessary.

Recommended LVDS Termination Circuit



LVDS TEST CIRCUIT

A single 100Ω termination resistor is needed. Some receiver ICs may include the resistor internally.

Signal Level Comparison