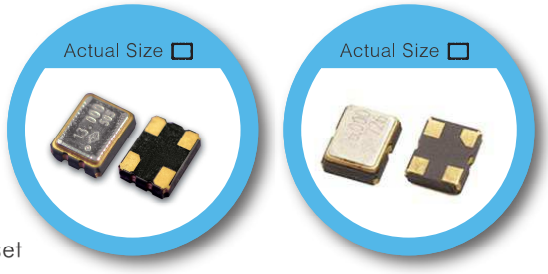
TX-J/TY-J Type

3.2 x 2.5 / 2.5 X 2.0 mm SMD CMOS Temperature Compensated Crystal Oscillator



FEATURE

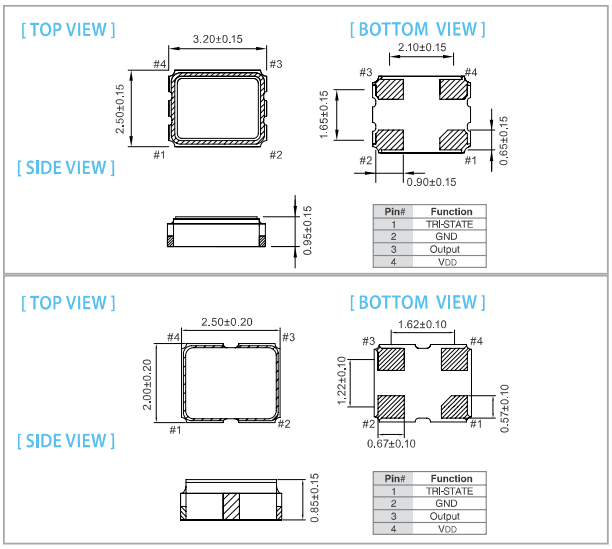
- Tolerance: ±2 ppm accuracy @25°C, ±2.5ppm over -40°C to +85°C-
- LVCMOS Output Logic
- Tight symmetry (45 to 55%) available.
- Operation voltage: 1.8V, 2.5V, 3.3V.
- Tri-state enable/disable.
- Femto second phase jitter and -145dBc/Hz at 10kHz offset

TYPICAL APPLICATION

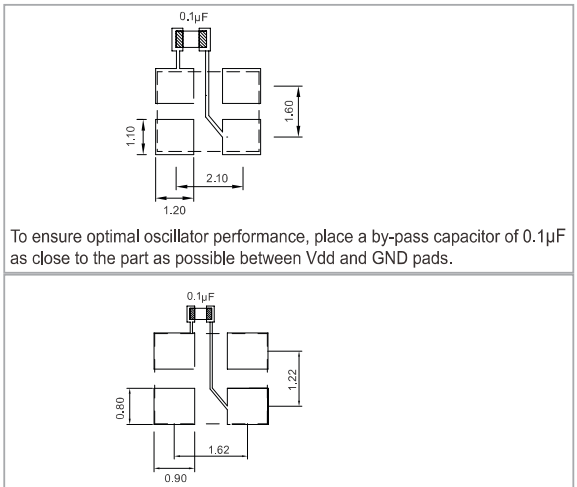
- Wireless Connectivity
- Smart grid

RoHS Compliant

DIMENSION (mm)



SOLDER PAD LAYOUT (mm)



To ensure optimal oscillator performance, place a by-pass capacitor of 0.1μF as close to the part as possible between Vdd and GND pads.

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ELECTRICAL SPECIFICATION

Parameter		3.3 V		2.5 V		1.8 V		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Supply Voltage Variation (VDD) ±5%		3.135	3.465	2.375	2.625	1.71	1.89	V
Frequency Range		9.5	60	9.5	60	9.5	60	MHz
Supply Current	9.5≦ Fo≦60 MHz	--	10	--	7	--	5	mA
Duty Cycle		45	55	45	55	45	55	%
Output Level (CMOS)	Output Hight(Logic"1")	2.97		2.25		1.62		V
	Output Low(Logic"0")		0.33		0.25		0.18	
Transition Time : Rise/Fall Time+			8		8		8	nSec
Start Time			5		5		5	mSec
Tri-State(Input to Pin 1)	Enable(High voltage or floating)	2.31		1.75		1.26		V
	Disable(Low voltage or GND)		0.99		0.75		0.54	
RMS Phase Jitter	(integrated 12kHz ~ 20MHz)		1		1		1	pSec
Phase Noise @ 26MHz	10Hz		-80		-80		-80	dBc/Hz
	100Hz		-110		-110		-110	
	1kHz		-130		-130		-130	
	10kHz		-145		-145		-145	
Aging (@25°C 1st year)			±1		±1		±1	ppm
Storage Temp. Range		-55	125	-55	125	-55	125	°C

Standard frequencies are frequencies which the crystal has been designed and does not imply a stock position
+Transition times are measured between 10% and 90% of VDD, with an output load of 15pF

FREQ. STABILITY vs. TEMP. RANGE

Temp. (°C) \ ppm	±2.5	±5.0	±10.0
-40 ~ +85	○	○	○
-40 ~ +90	△	○	○
-40 ~ +105	×	△	○

* ○: Available △:Conditional X: Not available

Note: not all combination of options are available. Other specifications may be available upon request.