TAITIEN
Our Performance Your Reputation

Ultra-High Precision Disciplined Oscillator DT-6565 series

Ultra-High Precision Disciplined Oscillator is a range of advanced clock modules which provide electrical timing functionality for telecommunication network systems to synchronize timing. These units primarily revolve around the 1PPS (pulse per second) timing synchronization signal and utilize the best performing oscillators with our proprietary algorithms to achieve the performance of atomic based oscillator.

Feature:

- ***24 Hours Holdover < 1.5uS, +/-10°C temperature change***
- 1pps input and 1pps output for 1pps synchronization
- Discipline to 1ns RMS in phase and $<10^{-12}$ in frequency
- 1 Second continuous phase measurement and report system, resolution ≦ 1ns
- ToD(Time of Day)
- RS232 digital interface
- 5MHz, 8.192MHz, 10MHz, HCMOS output
- -20°C ~ 70°C operating
- Proprietary adaptive algorithm

Applications:

- 5G Telecommunication, Base Station
- Smart Power Grid
- Test and measurement equipment

ELECTRICAL SPECIFICATIONS

1. RF OUTPUT

	Parameter		Min.	Typ.	Max.	Unit	Test Condition
1.1.	Frequency Output			10		MHz	5, 8.192MHz are available. Consult factory for other frequency
1.2.	Output Waveform			3.3V CMOS			Consult factory for another waveform
1.3.	Load			10MΩ//10pF			
1.4.	Rise/Fall Time				10	nS	
1.5.	Output Level	V_{OL}			0.4	V	
		V_{OH}	2.7				
1.6.	Duty Cycle		40		60		

	Parameter	Min.	Typ.	Max.	Unit	Test Condition
1.7.	Stability over Temperature			+/-0.1	ppb	-10°C ~ 70°C
1.8.	Frequency Accuracy			+/-1	$x10^{-12}$	24 hours average. Locked to 1pps.
1.9.	24Hours Holdover			1.5	uS	+/-10°C, after 7 days power on and 1 days discipline. Temperature variance below 1°C/Minute.
1.10.	Acceleration Sensitivity			+/-1	ppb/g	Worst direction, consult factory for better sensitivity.

2. 1pps Time Output

	Parameter	Min.	Typ.	Max.	Unit	Test Condition
2.1	1pps		1		Hz	
2.2	Output Amplitude		3.3V CMOS			
2.3	Pulse Width		20		us	
2.4	Rise/Fall Time			10	ns	
2.5	Load		10MΩ//10pF			

3. 1pps Time Input

	Parameter	Reference Std.	Test Condition
3.1.	1pps	1Hz	
3.2.	Timing Edge	Rising edge	
3.3.	Input Amplitude	3.3V CMOS	
3.4.	Input Impedance	10MΩ//10pF	

4. Phase Noise (@10MHz)

	Parameter	Min.	Typ.	Max.	Unit	Test Condition
4.1	1 Hz			-100	dBc/Hz	
4.2	10 Hz			-125	dBc/Hz	
4.3	100 Hz			-140	dBc/Hz	
4.4	1 KHz			-145	dBc/Hz	
4.5	10 KHz			-150	dBc/Hz	

5. Supply Voltage

	Parameter	Min.	Typ.	Max.	Unit	Test Condition
5.1	Supply Voltage	4.75	5.0	5.25	Vdc	
5.2	Steady Power			2.55	W	at 25°C ambient
5.3	Warm up Power			8.8	W	Factory configurable
5.4	Warm up Time			5	Min.	To +/-5ppb. Factory configurable for fast warm up

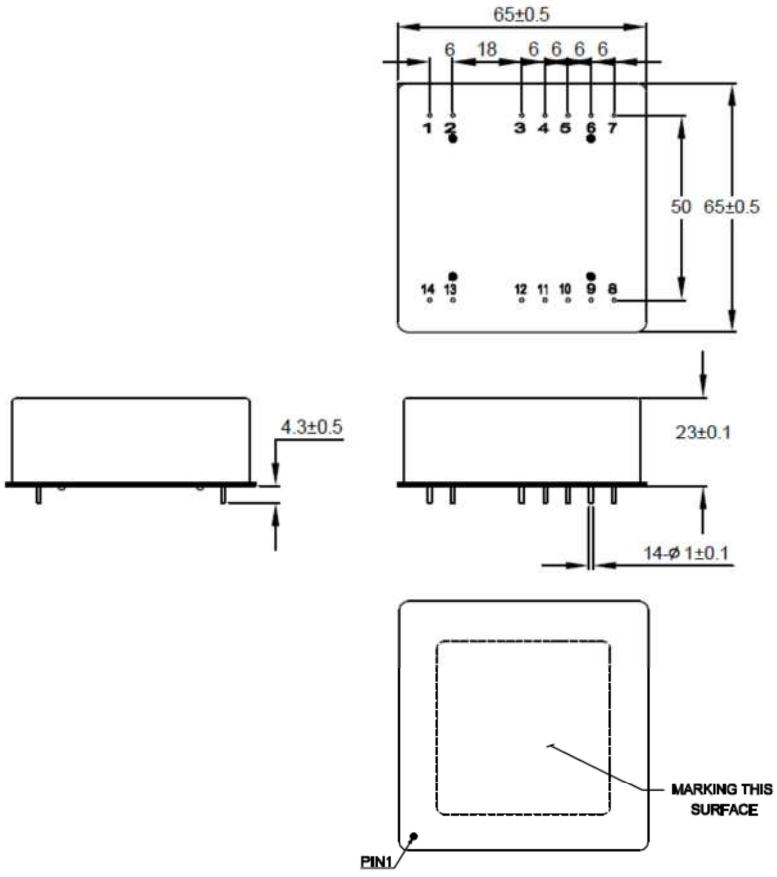
6. Digital Communication

	Parameter	Reference Std.	Test Condition
6.1.	Protocol	RS232	
6.2.	Logic Level	3.3V CMOS	
6.3.	Baud rate	57600 bps	

7. Environmental

	Parameter	Reference Std.	Test Condition
7.1.	Mechanical Shock	>30G, 11ms Half Sine	MIL-STD-202
7.2.	Vibration	5G up to 2KHz	MIL-STD-202

OUTLINE DRAWING



PIN DEFINITION			
PIN	Name		DESCRIPTION
2	10MHz OUTPUT		10MHz OCXO frequency output .
3	1PPS OUTPUT		The clock module 1PPS output.
5	State OUTPUT		State output.Output high level when the CM is locked and stable, others low level.
6	RX INPUT		Asynchronous serial data input.9600-N-8-1.
7	TX OUTPUT		Asynchronous serial data output.9600-n-8-1.
8	State INPUT	H:Lock Enable	The work state is set to normal operation when the state input is high level.
		L:Lock Disable	The module cannot be locked when the state input is low level.
10	1PPS INPUT		1PPS reference input.
12	VCC		Power supply input , 4.75V to 5.25V.
1、14	NC		Not connected.
4、9、11、13	GND		GND