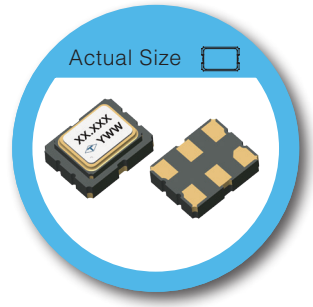
TX-U Type High Frequency and Low noise
3.2 x 2.5 mm Differential Output TCXO and VCTCXO



RoHS Compliant

FEATURE

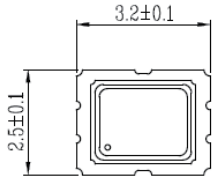
- Low Power Supply Voltage: 3.3, 2.5, and 1.8V supply options
- Clock Output: LVPECL, LVDS, CML, HCSL
- Output frequency support from 15MHz to 2.1GHz
- Ultra Low Phase RMS jitter :
  Typical: 150 fs at 12kHz to 20MHz frequency offsets
- Tri-state enable / disable mode.
- Temperature range: -40 to 85°C
- Pb-free/RoHS compliant

TYPICAL APPLICATION

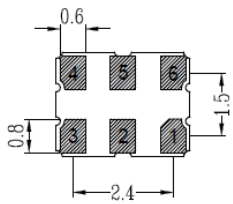
- 10/40/100 Gbps Ethernet, Fibre Channel SONET/SDH, Gigabit Ethernet.

DIMENSION (mm)

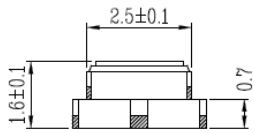
[TOP VIEW]



[BOTTOM VIEW]

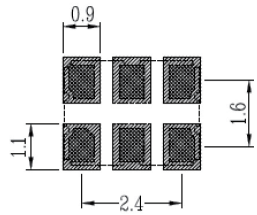


[SIDE VIEW]



NO	Name	Type	Function and Remarks
1	N.C.	-	For use in manufacturing plants only, connections may affect product characteristics
2	OE (Tri-state)	Input	Output control pin. Reference as below table Input level / Oscillation / Outputs "H" / Enable / Enable: Specified frequency "L" / Enable / Disable: Hi-Z
3	GND	Power-	GND pin
4	OUT	Output	Frequency output
5	$\overline{OUT}$	Output	Frequency output, inversion #4
6	V_{DD}	Power+	Power Supply, V_{DD} pin

SOLDER PAD LAYOUT (mm)



☆ To ensure optimal oscillator performance. Place a by-pass capacitor of 0.1 μF as close to the part as possible between VDD and GND pads.

ELECTRICAL SPECIFICATION LVDS OUTPUT

Parameter		LVDS 3.3V Min.	LVDS 3.3V Max.	LVDS 2.5V Min	LVDS 2.5V Max.	LVDS 1.8V Min	LVDS 1.8V Max.	Unit
Supply Voltage Variation (V_{DD})		3.63	2.97	2.25	2.75	1.71	1.89	V
Frequency Range		50	2100	50	2100	50	2100	MHz
Standard Frequency			50、100、125、155.52、156.25、212.5、312.5、625					MHz
Frequency Tolerance		-	±2.0	-	±2.0	-	±2.0	ppm
Frequency stability								
Vs Supply Voltage(±5%) change			±0.2		±0.2		±0.2	ppm
Vs Aging (First year)			±0.2		±0.2		±0.2	ppm
Supply Current		-	90	-	80	-	70	mA
Output Level	Output High	-	1.6	-	1.6	-	1.6	V
	Output Low	0.9	-	0.9	--	0.9	-	V
Transition Time	Rise Time	-	0.35	-	0.35	-	0.35	nSec
(20% - 80%)	Fall Time	-	0.35	-	0.35	-	0.35	nSec
Duty Cycle		45	55	45	55	45	55	%
Startup Time		-	8	-	8	-	8	mSec
Tri-State mode	Enable	0.7 x V_{DD}	-	0.7 x V_{DD}	-	0.7 x V_{DD}	-	V
(Input to Pin 2)	Disable	-	0.3 x V_{DD}	-	0.3 x V_{DD}	-	0.3 x V_{DD}	V
Stand by Current		-	90	-	80	-	70	mA
Phase Noise		Typ.	Max.	Typ.	Max.	Typ.	Max.	
	1kHz offset	-106	-	-106	-	-106	-	dBc/Hz
At VDD=3.3V,	10kHz offset	-115	-	-115	-	-115	-	dBc/Hz
fout=	100kHz offset	-123	-	-123	-	-123	-	dBc/Hz
873.515MHz	1MHz offset	-133	-	-133	-	-133	-	dBc/Hz
	10MHz offset	-150	-	-150	-	-150	-	dBc/Hz
RMS Phase Jitter (12KHz to 20MHz)		150	250	150	250	150	250	fs
Period Jitter		-	50	-	50	-	50	ps

Note: not all combination of options are available. Other specifications may be available upon request.

ELECTRICAL SPECIFICATION LVPECL OUTPUT

Parameter		LVPECL				Unit
		3.3V		2.5V		
		Min.	Max.	Min.	Max.	
Supply Voltage Variation (V_{DD}) ± 10%		2.97	3.63	2.25	2.75	V
Frequency Range		50	2100	50	2100	MHz
Standard Frequency		50、100、125、155.52、156.25、212.5、312.5、625				MHz
Frequency Tolerance		-	±2.0	-	±2.0	ppm
Frequency stability						
Vs Supply Voltage(±5%) change			±0.2		±0.2	ppm
Vs Aging (First year)			±0.2		±0.2	ppm
Supply Current		-	110	-	95	mA
Output Level	Output High	V_{DD} - 1.165	V_{DD} - 0.8	V_{DD} - 1.165	V_{DD} - 0.8	V
	Output Low	V_{DD} – 2.0	V_{DD} – 1.55	V_{DD} – 2.0	V_{DD} – 1.55	V
Transition Time (20% - 80%)	Rise Time	-	0.35	-	0.35	nSec
	Fall Time	-	0.35	-	0.35	nSec
Duty Cycle		45	55	45	55	%
Startup Time		-	8	-	8	mSec
Tri-State mode	Enable	0.7 x V_{DD}	-	0.7 x V_{DD}	-	V
(Input to Pin 2)	Disable	-	0.3 x V_{DD}	-	0.3 x V_{DD}	
Stand by Current		-	110	-	95	mA
Phase Noise		Typ.	Max.	Typ.	Max.	
At VDD=3.3V, fout= 873.515MHz	1kHz offset	-106	-	-106	-	dBc/Hz
	10kHz offset	-115	-	-115	-	dBc/Hz
	100kHz offset	-123	-	-123	-	dBc/Hz
	1MHz offset	-133	-	-133	-	dBc/Hz
	20MHz offset	-150	-	-150	-	dBc/Hz
RMS Phase Jitter (12KHz to 20MHz)		150	250	150	250	fs
Period Jitter		-	50	-	50	ps

ELECTRICAL SPECIFICATION HCSL OUTPUT

Parameter		HCSL						Unit
		3.3V		2.5V		1.8V		
		Min.	Max.	Min	Max.	Min.	Max.	
Supply Voltage Variation (V_{DD})		3.63	2.97	2.25	2.75	1.71	1.89	V
Frequency Range		15	700	15	700	15	700	MHz
Standard Frequency		50、100、125、155.52、156.25、212.5、312.5、625						MHz
Frequency Tolerance		-	±2.0	-	±2.0	-	±2.0	ppm
Frequency stability								
Vs Supply Voltage(±5%) change			±0.2		±0.2		±0.2	ppm
Vs Aging (First year)			±0.2		±0.2		±0.2	ppm
Supply Current		-	90	-	80	-	70	mA
Output Level	Output High	0.66	1.15	0.66	1.15	0.66	1.15	V
	Output Low	0	0.15	0	0.15	0	0.15	V
Transition Time	Rise Time	-	0.35	-	0.35	-	0.35	nSec
(20% - 80%)	Fall Time	-	0.35	-	0.35	-	0.35	nSec
Duty Cycle		45	55	45	55	45	55	%
Startup Time		-	8	-	8	-	8	mSec
Tri-State mode	Enable	0.7 x V_{DD}	-	0.7 x V_{DD}	-	0.7 x V_{DD}	-	V
(Input to Pin 2)	Disable	-	0.3 x V_{DD}	-	0.3 x V_{DD}	-	0.3 x V_{DD}	V
Stand by Current		-	90	-	80	-	70	mA
Phase Noise		Typ.	Max.	Typ.	Max.	Typ.	Max.	
At VDD=3.3V, Fout= 805.664MHz	1kHz offset	-107	-	-107	-	-107	-	dBc/Hz
	10kHz offset	-117	-	-117	-	-117	-	dBc/Hz
	100kHz offset	-125	-	-125	-	-125	-	dBc/Hz
	1MHz offset	-135	-	-135	-	-135	-	dBc/Hz
	20MHz offset	-150	-	-150	-	-150	-	dBc/Hz
RMS Phase Jitter (12KHz to 20MHz)		150	250	150	250	150	250	fs
Period Jitter		-	50	-	50	-	50	ps

ELECTRICAL SPECIFICATION CML OUTPUT

Parameter		CML						Unit
		3.3V		2.5V		1.8V		
		Min.	Max.	Min	Max.	Min.	Max.	
Supply Voltage Variation (V_{DD})		3.63	2.97	2.25	2.75	1.71	1.89	V
Frequency Range		15	2100	15	2100	15	2100	MHz
Standard Frequency		50、100、125、155.52、156.25、212.5、312.5、625						MHz
Frequency Tolerance		-	±2.0	-	±2.0	-	±2.0	ppm
Frequency stability								
Vs Supply Voltage(±5%) change			±0.2		±0.2		±0.2	ppm
Vs Aging (First year)			±0.2		±0.2		±0.2	ppm
Supply Current		-	90	-	80	-	70	mA
Output Level	Output High	V_{DD} - 0.085	V_{DD}	V_{DD} - 0.085	V_{DD}	V_{DD} – 0.085	V_{DD}	V
	Output Low	V_{DD} – 0.6	V_{DD} – 0.32	V_{DD} – 0.6	V_{DD} – 0.32	V_{DD} – 0.6	V_{DD} – 0.32	V
Transition Time	Rise Time	-	0.35	-	0.35	-	0.35	nSec
(20% - 80%)	Fall Time	-	0.35	-	0.35	-	0.35	nSec
Duty Cycle		45	55	45	55	45	55	%
Startup Time		-	8	-	8	-	8	mSec
Tri-State mode	Enable	0.7 x V_{DD}	-	0.7 x V_{DD}	-	0.7 x V_{DD}	-	V
(Input to Pin 2)	Disable	-	0.3 x V_{DD}	-	0.3 x V_{DD}	-	0.3 x V_{DD}	V
Stand by Current		-	90	-	80	-	70	mA
Phase Noise		Typ.	Max.	Typ.	Max.	Typ.	Max.	
At VDD=3.3V, Fout= 805.664MHz	1kHz offset	-107	-	-107	-	-107	-	dBc/Hz
	10kHz offset	-117	-	-117	-	-117	-	dBc/Hz
	100kHz offset	-125	-	-125	-	-125	-	dBc/Hz
	1MHz offset	-135	-	-135	-	-135	-	dBc/Hz
	20MHz offset	-150	-	-150	-	-150	-	dBc/Hz
RMS Phase Jitter (12KHz to 20MHz)		150	250	150	250	150	250	fs
Period Jitter		-	50	-	50	-	50	ps

Freq. Stability vs. Temp. Range

ppm / Temp. (°C)	±1.0	±2.0	±2.5	±5.0
-20~+70	O	O	O	O
-40~+85	O	O	O	O
-40~+105	X	△	△	O

* O: Available △:Conditional X: Not available

*Inclusive of calibration @ 25°C, operating temperature range, input voltage variation, load variation, aging (1st year), shock, and vibration

Phase Noise Test Data

VDD=3.3V, LVPEL OUTPUT, 312.500000MH->Phase RMS jitter: 158.8fsec